Hardware Acceleration for Sensor Data Fetch

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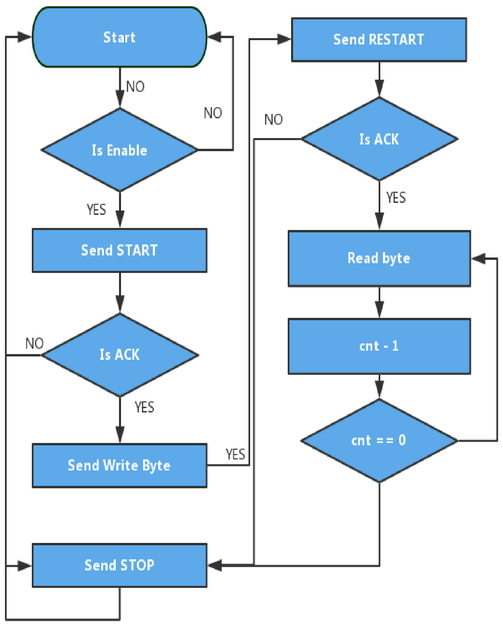
Introduction

PROBLEM:

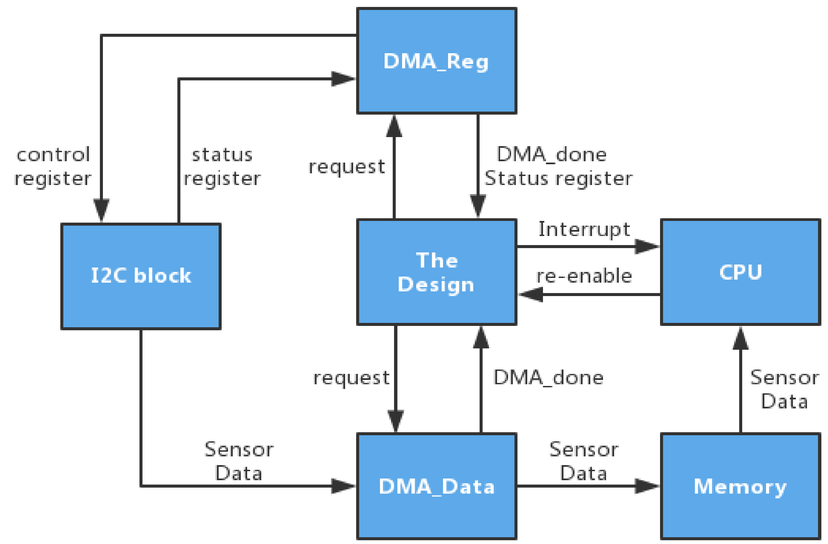
- Sensor data fetch slow via I2C
- I2C processing consumes a lot of CPU time
- Computational resource is limited in real-time system like robot.

GOAL: Design a logic hardware to parallelize the sensor data fetch and save CPU time for high-level compute-intensive algorithms like data fusion.

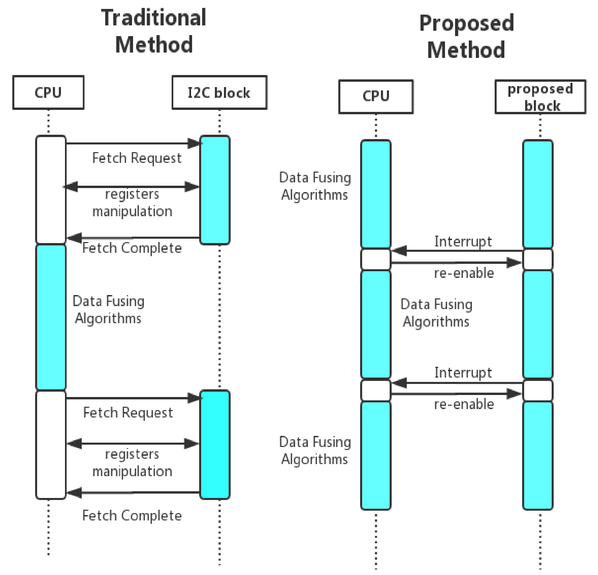


Hardware Design

- Use DMA (Direct Memory Access) to apply the change to control register, read status register and transfer sensor data to Memory
- Use UDB (Universal Digital Block) on pSoC5LP to design the logic hardware
- Follow the fixed routine of sensor data fetch via I2C



Experiment Result



- Performance tested on pSoC5LP with a MPU9250 and four hall sensors
- Reduce CPU intervention time from 2000 us to 5 us
- Sample rate doubles
- Works well with multiple sensors

Discussion

This design has the potential to be integrated into any general I2C block as a new IP core in a SoC so that sensor data fetch, especially in a multi-sensor system, does not affect a system to be real-time

Acknowledgement

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